Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CP1**
2. **MR1**
3. **Q0A**
4. **Q1A**
5. **Q2A**
6. **Q3A**
7. **GND**
8. **Q3B**
9. **Q2B**
10. **Q1B**
11. **Q0B**
12. **MR2**
13. **CP2**
14. **VCC**

**2 1 14 13 12**

**3**

**4**

**5**

**6 7 8**

**11**

**10**

**9**

**A13N**

**LS393**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: A13N LS393**

**APPROVED BY: DK DIE SIZE .054” X .068” DATE: 10/7/21**

**MFG: MOTOROLA THICKNESS .014” P/N: 54LS393**

**DG 10.1.2**

#### Rev B, 7/1